AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

(a) receiving a vertical synchronizing signal;

(b) receiving a data enable signal DE which has a vertical blank period;

~~(b)~~ (c) generating a gate clock signal CPV which has a plurality of gate clock cycles C1-Cn;

~~(c)~~ (d) after a rising edge or a falling edge of the vertical synchronizing signal, generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of the gate clock signal CPV; ~~and~~

~~(d)~~ (e) after a rising edge or a falling edge of the vertical synchronizing signal, generating start vertical signals STV before the end of the vertical blank period VB and after at least a gate clock cycle C1 during the vertical blank period VB; and

(f) pausing output of CPV, STV, and OE until the end of the vertical blank period VB.

2. (Original) The method as claimed in claim 1, wherein in the step (c), start vertical signals STV are generated after at least a third cycle C3 during the vertical blank period VB.

3. (Cancelled)

4. (Original) The method as claimed in claim 1, wherein the start vertical signals STV includes:

a first start vertical signal STV1, for determining a start scan location of a frame; and

a second start vertical signal STV2, for offsetting flicker and display brightness of the liquid crystal display.

5. (Cancelled)

6. (New) A method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

(a) receiving a data enable signal DE;

(b) decoding the signal to generate a vertical synchronizing signal;

(c) generating a gate clock signal CPV which has a plurality of gate clock cycles C1-Cn;

(d) after a rising edge or a falling edge of the vertical synchronizing signal, generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of the gate clock signal CPV;

(e) after a rising edge of a falling edge of the vertical synchronizing signal, generating start vertical signals STV before the end of the vertical blank period VB and after at least a gate clock cycle C1 during the vertical blank period VB; and

(f) pausing output of CPV, STV, and OE until the end of the vertical blank period VB.

7. (New) The method as claimed in claim 6, wherein in step (c), start vertical signals STV are generated after at least a third cycle C3 during the vertical blank period VB.

8. (New) The method as claimed in claim 6, wherein the start vertical signals STV include:

a first start vertical signal STV1, for determining a start scan location of a frame; and

a second start vertical signal STV2, for offsetting flicker and display brightness of the liquid crystal display.